7.2 A 64Mb Chain FeRAM with Quad-BL Architecture and 200MB/s Burst Mode

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A 64Mb chainFeRAM™ is fabricated using 0.13μm 1P3M CMOS technology. A quad-BL architecture with combination of folded and shielded BLs eliminates BL-BL coupling noise, and reduces die size by 6.5% and power consumption by 28%. A high-speed ECC circuit and cell-data write-back scheme satisfy both high reliability and high-speed read/write of 60ns cycle time and 200MB/s burst. The chip size is 87.5mm^2 with an average cell size of 0.7191μm^2.

In mobile applications, a non-volatile memory that satisfies not only high density and low power, but also a high-speed and high-bandwidth interface is required. In this paper, a 64Mb chain FeRAM with high-bandwidth 200MB/s burst is presented. A chain-FeRAM architecture realizes small die with high cell-efficiency and high speed [1, 2]. In a 64Mb chain FeRAM, the BL pitch is shrunk to 0.68μm. BL-BL coupling noise becomes a severe problem, even in cross-point-type chain cell [1]. A quad-BL architecture minimizes BL-BL coupling noise without any area and process penalty and also reduces the sense-amp area and power consumption. Moreover, the chip adopts high-speed ECC circuit in order to satisfy high reliability even at severe operating conditions, such as high-temperature operation and many read/write cycles, to meet the requirements of high-end applications.

Figure 7.2.1(a) illustrates the quad-BL architecture. The proposed scheme has the advantages of both folded- and shielded-BL architectures. One sense amplifier is shared with two BL pairs. This reduces the sense-amplifier area to half. One of the two BL pairs is coupled with sense amplifier. The other, which is kept at pre-charge voltage V_{ref}, acts as a shield and eliminates BL-BL coupling noise. Although conventional BL-BL noise-reduction techniques require extra twist area or layer for shield [3], the proposed quad-BL architecture has no area penalty or extra layer.

Figure 7.2.1(a) shows the case that the ferroelectric capacitor C1 is selected and the cell data is read out to bitline /BL0 while BL0 acts as reference bitline, other /BL1 and BL1 act as shield. The easy way to realize folded and shielded BLs is to introduce four kinds of block-selecting transistors and activate one of four to connect the cell to the bitline. However, this causes a larger chain block. The proposed chain block realizes quad-BL by introducing only two kinds of block-selecting signals, BS0 and BS1, although four kinds of platelines are needed (this problem is discussed later). By designing plateline precharge level to be the same as BL precharge level, no bias is applied to the memory cell, and the data of capacitor C2 is not destroyed even when the block-selecting transistor Q1 is turned on, as shown in /BL1 of Fig. 7.2.1(a).

The area penalty of introduction of four kinds of platelines is also solved. In 0.13μm node, the minimum M3 pitch is still tighter than the memory-cell pitch. Therefore, there is enough space to run four platelines of M3 per two chain blocks in addition to the M3 lines used for stitching WLs as shown in the cross-section and layout of Fig. 7.2.1(b).

The proposed scheme reduces BL-BL noise to 4.5%, the die size by 6.5%, and the power consumption by 28%, because the number of sense amplifiers and activated BLs are both reduced to half.

To realize fast ECC calculation and fast cycle time, two design techniques are introduced; a fast pre-parity calculation ECC scheme and a pseudo-"0"-write-before-data-write scheme.

To minimize the memory array used for parity bit, the chip adopts an internal bus of 72b ECC word using 8b parity for 64b data, whereas the chip I/O is 16b wide. By this mismatch, the 48b data that is read out from the cell and corrected by ECC, in addition to the 16b data from I/O, must be used as write-back data. This causes a complex 3-step ECC sequence: (1) syndrome generation, (2) readout data correction using syndrome, and (3) parity generation using corrected data and external I/O data in order to write back to the memory cell.

On the other hand, the proposed ECC circuit reduces the calculation steps to 2/3 as shown in Fig. 7.2.2. In the first step, parity bits to write back to memory cells are previously calculated whether data read out from the memory cell is correct or not. At the same time, the syndrome is generated to correct the memory cell data. After that, pre-parity data is corrected by using syndrome data when pre-parity data is wrong, and data is also corrected in parallel. The scheme reduces the total ECC calculation time by 27%.

Even by applying the proposed ECC scheme, the write-back operation can not start until corrected data is obtained by ECC. In the conventional FeRAM, the valid data from ECC circuit in peripheral must come back to the sense amplifier before the plateline is pulled down, because "0" data can be written only when the plateline is high. After that, "1" data is written after the plateline is low. Therefore, the introduction of ECC causes cycle-time delays in the ECC path; data read from the array to the peripheral, ECC calculation, and data write from the peripheral to the array.

Pseudo-"0"-write-before-data-write scheme enables earlier data write-back as shown in Fig. 7.2.3(a). First, readout data is transferred to the peripheral. Then "0" data is written for selected columns while the plateline is kept at high, and the plateline is pulled down immediately. At the same time, readout data is transferred to ECC circuit and readout data is corrected. After plateline becomes low, the corrected data is written back to the memory cell. The proposed scheme reduces ECC time penalty, because final data derived from ECC can be written even after the plateline is low, since "0" data is already written when the plateline is high. Fig. 7.2.3(b) shows cycle-time comparison. This work reduces ECC time by 2ns and write-back time by 6ns, and reduces the total cycle time from 68ns to 60ns.

Figure 7.2.4 shows the simulated waveforms of burst-write operation with ECC. The external 16b data are fetched in input buffers at 100MHz, and 64b data fetched by 4 clocks are simultaneously transferred to the memory cell via ECC circuit within four 10ns column cycles. A 200MB/s data throughput rate is achieved for both read and write operations.

Figure 7.2.5 shows the micrograph of the 64Mb chain FeRAM fabricated in 0.13μm CMOS technology. The average cell size is 0.7191μm^2. The chip size is 87.5mm^2. The cell efficiency of 55.2% with ECC (equivalent to 62% without ECC) is achieved. The device features are summarized in Fig. 7.2.6.

References:

[1] D. Takashima, et al., "A 76-mm^2 8-Mb Chain Ferroelectric Memory," *IEEE J. Solid-State Circuits*, vol. 36, no. 11, pp. 1713-1720, Nov., 2001.

[2] S. Shiratake, et al., "A 32Mb Chain FeRAM with Segment / Stitch Array Architecture," *IEEE J. Solid-State Circuits*, vol. 38, no. 11, pp. 1911-1919, Nov., 2003.

[3] K. Yamaoka, et al., "A 0.9-V 1T1C SBT-Based Embedded Nonvolatile FeRAM With a Reference Voltage Scheme and Multilayer Shielded Bit-Line Structure," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 286-292, Jan., 2005.

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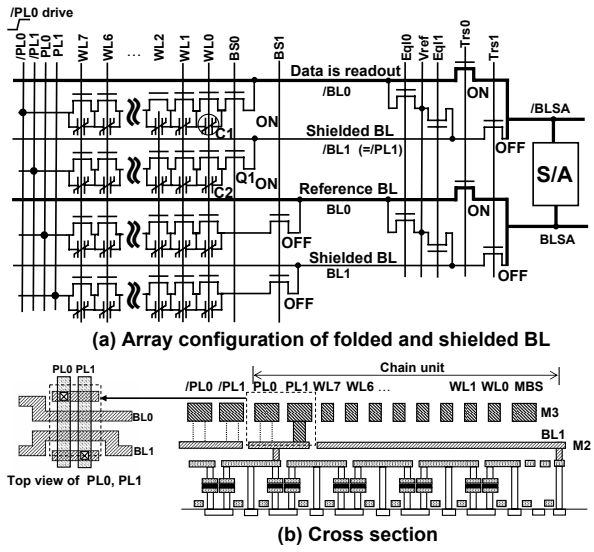

Figure 7.2.1: Quad-BL architecture.

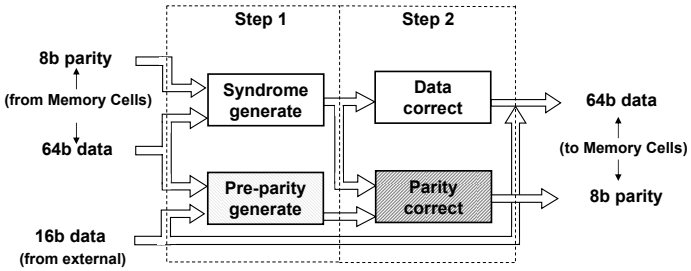

Figure 7.2.2: Fast pre-parity calculation ECC sequence in write operation.

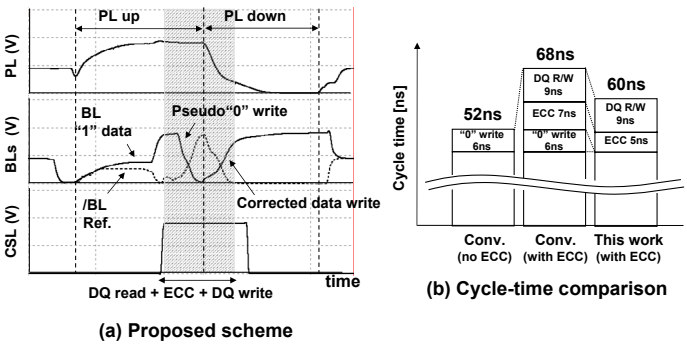

Figure 7.2.3: Pseudo-"0"-write-before-data-write scheme for canceling ECC time penalty.

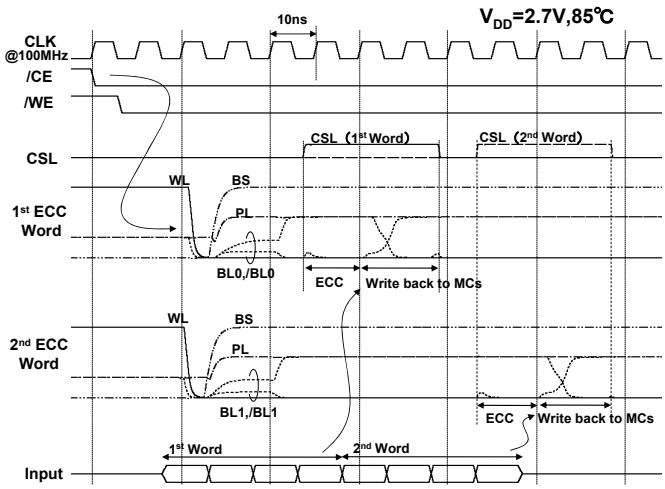

Figure 7.2.4: 200MB/s burst write with ECC.

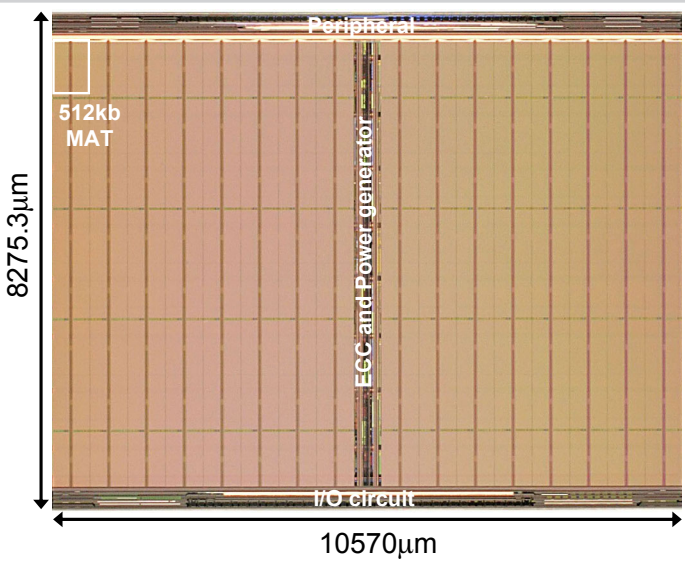

Figure 7.2.5: 64Mb chain FeRAM chip micrograph.

Technology:

0.13µm 1P3M CMOS
Cell Size (Ave.)=0.7191µm^2
Chip Size=87.5mm^2

Performance:

Supply Voltage=3.3V/2.7V
Active Current=58mA at t_{RC}=60ns
Cycle Time=60ns@85°C (w/ ECC)
Standby Current=8µA

Interface:

/CE Control, CLK Control with 200MB/s Burst

Figure 7.2.6: 64Mb chain FeRAM features.